Complete DMT ADSL Chipset

a

Preliminary Technical Information   AD20msp910

FEATURES:

Complete Chipset for DMT based
        Asymmetric Digital Subscriber Loop (ADSL)
Suitable for either ATU-C or ATU-R
Designed to ANSI T1.413 / ETSI TR238 / ITU G.adsl
        (Category 1 - FDM) Standards
Typical performance over CSA loop:
        6Mbps downstream, 224Kbps duplex.
        Also supports user-defined data-rates
        (eg 4Mbps/512Kbps for Internet access, or
        1.5M/224Kbps for long reach)
        Absolute maximum 12Mbps/2Mbps
Supports rate adaption & variable data rates (32Kbps
        steps) to optimize performance in loop reach/
        rate trade-off
Complete software control protocol stack/API
Implements many features of Issue 2
Meets strict psd mask requirements (exceeds Issue 2)
Complete Data-pump in five compact ICs:
        Three 128TQFP, One 80PQFP, one VR15
Power: 1.9 W   (excl. driver & signal)
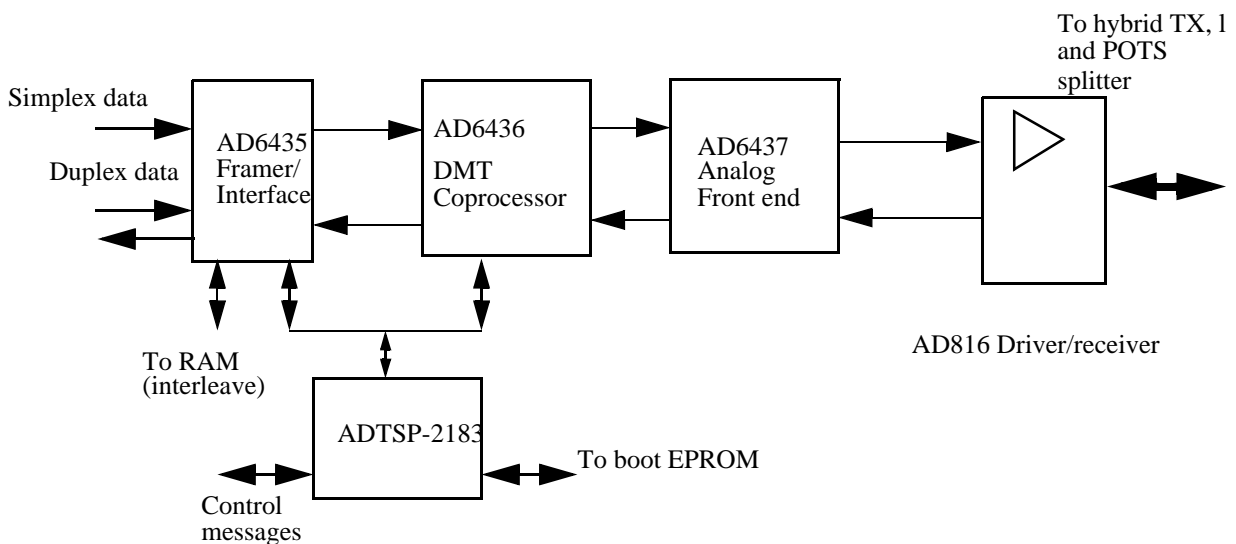**-40 to + 85 C operation**

GENERAL DESCRIPTION

This is a complete chipset for implementing ADSL modems, designed to ANSI T1.413 / ETSI standard (Category 1 - FDM). It includes all components, including controller, the analog front-end, driver/receiver and all software. The same chipset is used at CO and RT.

The AD20msp910 uses the standard DMT modulation method, which is highly resistant to noise and supports rate adaption to deliver optimum performance over any loop. For example, the standard performance is 6Mbps/224Kbps over 12,000 feet, but the modem will easily reach more on shorter lengths (absolute max is 12Mbps downstream & 2Mbps duplex), or achieve longer reaches at reduced rate.

This chipset is a complete solution, containing framer, DMT transceiver, analog components (driver, receiver, filter) and control processor. Also supplied is object code software for both modem and a complete set of management / control functions (API or protocol stack) that is a superset of those defined in T1.413, and handles all real-time functions (including all performance logging & statistics gathering). The chipset also implements many features of Issue 2 of the standard.

This complete solution reduces development time & risk for system designers.

Simplex data →
Duplex data →
AD6435 Framer/ Interface → **AD6436 DMT Coprocessor** → **AD6437 Analog Front end** → To hybrid TX, l and POTS splitter

AD816 Driver/receiver

To RAM (interleave)

ADTSP-2183 → To boot EPROM

Control messages

Revision 0.6 (23 Mar 97)   **1**   **ADI Proprietary**

Table 1. ADSL Category 1 MODEM SPECIFICATIONS

SPECIFICATION	VALUE	UNITS	COMMENTS
Absolute Maximum Data Rates Downstream Duplex	 12.288 2.048	 Mbps Mbps	Actual performance is primarily limited by loop noise and crosstalk. These figures apply at best-case loops, where the limit is a function of data-packing and interfacing.
Typical Payload Data Rate T1.601 Downstream Duplex	 1.544 224	 Mbps Kbps	Loop set T1.601 (7,13) eg approximately 13,500 ft. of 26 AWG (4.2km of 0.4mm) Configuration can vary depending on FDM split & bin assignments. This configuration corresponds to the default requirements of T1.413
Typical Payload Data Rate - CSA Downstream Duplex	 6.144 224	 Mbps Kbps	Loop set CSA (4,6,7) & mid-CSA eg 12,000 ft. of 24 AWG (3.7 am of 0.5mm) Other configurations are possible, under software control.
ADSL overhead Downstream Duplex	 192 96	 kbps kbps	
DS Bandwidth	0.11-1.1	MHz	Category 1 - frequency division multiplexing. of up & downstream signals. POTS is located in Bin 0 (0-4kHz). Till 30kHz is guard band for filters. Typical allocation is bins 8-19 for upstream, 20-255 for downstream.
US Bandwidth	30-85	kHz	
DS TX Power	23	dBm	Can support power boost
US TX Power	12	dBm	Can be boosted to 15dBm
Bin Width	4.3125	kHz	As specified in T1.413, tolerance +/- 50ppm
Max Symbols/Bin	16 bits		Actual loading depends on SNR of sub-band Bit swapping is supported. NB This is better than the 15 required in T1.413
Latency: Fast Channel Interleaved channel	 <2 <20	 ms ms	

Table 2.   - Bill Of Materials of ADSL Generation 2

PART NO.	NAME	DESCRIPTION	Qty	PACK-AGE	POWER
AD6435XST	**DTIR**	**Digital Interface IC. Implements Inter-face & Elastic store operations, error-correction/detection etc.**	**1**	**128TQFP**	**600mW 180mA, 3.3V**
AD6436XST	**DME**	**Discrete Multitone Engine. Performs all the core DSP operations of DMT.**	**1**	**128TQFP**	**750mW 227mA, 3.3V**
AD6437XS	**AFIC**	**Complete single-chip analog front end IC. Integrates ADC, DAC, PGA, filters and support analog circuitry.**	**1**	**80PQFP**	**400mW 50mA, 5V**
ADTSP-2183BST-115	**DSP**	**16-bit general purpose fixed-point DSP, with 80K internal RAM; 3V version of ADTSP-2181. Used for training opera-tions, and as general purpose controller in system.**	**1**	**128TQFP**	**250mW 76mA, 3.3V**
Op-amps	**HPF, BPF**	**CO: AD8042AR x 3; AD826AR x 1 RT: AD8042AR x 2; AD8072JR x 1**	**Co: 4 RT:3**	**8SOIC**	**30mW 6mA, 5V**
AD816AVR	**DRIVER /Receiver**	**+26dBm low distortion, high bandwidth line driver. Also includes two op-amps used in the receive-side hybrid network.**	**1**	**VR15 Surface mount DDPAK**	**2.5W @CO 2.1W @RT NB Depends on rate**

All of these ADI components are included in the chipset.

Table 3.   Example Non-ADI Parts Needed

DESCRIPTION	Qty	EXAMPLE PART
32Kx8, 3.3V fast CMOS SRAM Interleave memory. Not required if interleave path is disabled.	**1**	**IDT71V256SA**
35MHz VCXO	**1**	**Champion Technologies K1523BA (At RT only)**
Boot EPROM	**1**	
Wideband transformer in hybrid	**1**	**AT&T 2718AF**
Passives (for filters, decoupling etc)		

These parts or equivalents are required to complete the modem, and are included in the reference design, but are not part of the ADI chipset. They are listed here for completeness.

Table 4. Power Requirements: ATU-C

	Digital	Analog	Analog
Part #	3.3V	5V	+/-15V
AD6435	0.60		
AD6436	0.75		
ADSP2183	0.25		
AD6437		0.40	
AD8042		0.03	
Core chipset	**1.60**	**0.43**	**0.00**
AD816			1.00
Subtotal	**1.60**	**0.43**	**1.00**
SIGNAL		0.16	1.44
Supply Power	**1.60**	**0.59**	**2.44**
Total Power	**4.63**		

Table 5. Power Requirements: ATU-R]

	Digital	Analog	Analog
Part #	3.3V	5V	+/-15V
AD6435	0.60		
AD6436	0.75		
ADSP2183	0.25		
AD6437		0.50	
AD8042		0.07	
AD812		0.04	
Core Chipset	**1.60**	**0.61**	**0.00**
AD816			1.00
Subtotals	**1.60**	**0.61**	**1.00**
SIGNAL		0.12	1.08
Supply Power	**1.60**	**0.73**	**2.08**
Total Power	**4.41**		

Figures are Watts

These power budgets are for worst case (maximum data rate / maximum reach) cases, using power levels as specified in T1.413. In many cases, actual implementations will require lower power consumption, for example if a lower data rate was used.
For lower data rates, the power dissipation in the driver (AD816) can be reduced dramatically by reducing the supply voltage. At the ATU-R, with its lower upstream rate, this would allow operation off, say, a +/- 12V or even lower rail.

 In addition, system design may reduce power - eg with power-down or "sleep" options.

Figure 1.   System Block Functional Diagram
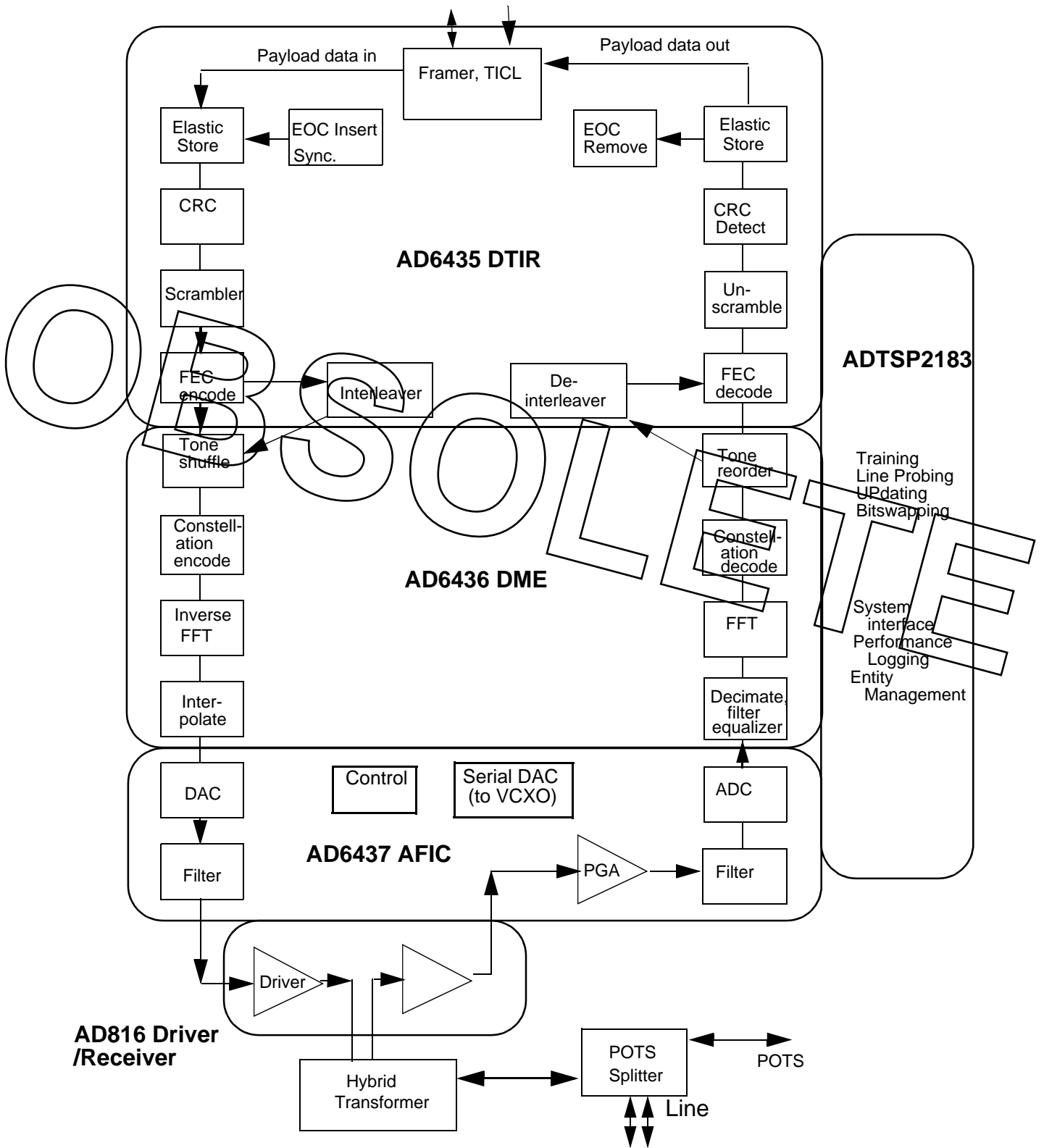
SYSTEM DESCRIPTION

The ADSL chipset is optimized for ANSI T1.413 compliant systems. It consists of: two dedicated digital ICs, one which handles the digital interfacing & processing, the other for the core DMT functionality; a single-chip analog front end, integrating all the mixed-signal and analog signal processing into one package; a power driver/receiver and a general-purpose 16-bit DSP, used for training but available for system management & control tasks. Firmware from Aware implements high performance signal processing algorithms needed for category 1 ADSL operation. The chipset includes all the silicon required for an ADSL datapump; however it does not include the system control functions, framer or POTS splitter - these are system specific and the realm of the OEM.

This is a Category 1 modem. The upstream and downstream bands are separated using FDM. The chipset is rate adaptive, and depending on software mode settings, can optimize data rate to suit a given loop. However, the allocation of tones to upstream or downstream must be done in hardware. Many configurations can be supported, controlled by software settings and analog filter values. Some typical ones are:

      6.1Mbps / 224Kbps over CSA loop (Based on T1.413 standard)
      1.5 Mbps / 192 Kbps (optimized for extended range & margin)
      4Mbps / 512Kbps over CSA loop (more suited to data services & Internet access)
      (NB   TCP/IP requires a typical asymmetry of no more than 10:1 between down/up stream data to allow for acknowledgment packets. Use of too small an upstream may 'choke' the downstream).

The maximum rate will be determined by the loop environment and crosstalk. The chipset has absolute maximum rates of 12Mbps duplex and 2Mbps on the duplex link. These will be limited by the channel (attenuation, noise, crosstalk) rather than the chipset and these rates would be achieved only on very short loops (detailed simulations are provided in Figures 3-6). The AD6435 interface IC supports rates of up to 12Mbps on the simplex, and 4Mbps on the duplex streams; this is to allow for future developments that will allow more upstream tones.

Although described as having a simplex and duplex channels (in which case these correspond to AS0 and LS0 of T1.413), a more accurate description is that there are three independent channels: one high speed downstream, one medium speed downstream, and a medium speed upstream. There is no requirement that the two data rates on the "duplex" be the same - or even that both be used. For example, in a networking application, the medium speed downstream may be redundant and not connected.

The split between up and (total) downstream is determined by filters in the analog stage (eg bins 8-20 are used for US, bins 21-255 for downstream).   Given that, the exact rate is established on configuration, according to the control information passed to the DSP.

In conventional ADSL implementations, the lower 8 bins (0-7) are reserved for analog POTS and a filter roll-off. However, it is possible to change this, and the AD20msp910 will automatically adapt. Two typical examples would be:
no-POTS operation, using a dedicated copper line for data, and using all bins from 0 up to increase upstream traffic;
or using fewer bins and starting at a higher frequency in order to support an ADSL over ISDN application.

DIGITAL SECTION

There are three components in the digital section:
AD6435 DTIR
AD6436 DME
ADTSP-2183

AD6435 DTIR

TheAD6435 interfaces the ADSL modem to the external system, at either CO or RT modem.
It has two separate sections:

* The TICL (transfer, interface control logic) implements the interfacing & buffering operations, including the bit-stuffing/robbing, elastic store, FIFO etc.

* The DIA (digital interface area) implements the error correction/detection and interleaving operations (this section is essentially the same as the earlier AD6442 DIA circuit).

The AD6435 has four simple synchronous connections, simplex (downstream) in & out, and duplex in and out. These have "clean" clock and data, and may operate asynchronously of one another, or of the modem itself.
The "duplex" streams can be treated as such, or can operate independently, with asynchronous clocks and data rates.
(At the ATU-C the simplex out is not used, and conversely simplex in is unused at ATU-R).

The TICL section of the DTIR performs interface signal buffering and timing recovery functions. This function is complicated by the asynchronicity of the simplex and duplex data streams from the modem clock and from each other. The role differs depending on whether it is in CO or RT mode. For downstream transmission in CO mode, payload input data is clocked directly into a FIFO and the data is subsequently read out from the FIFO and multiplexed into the outgoing ADSL frames. This operation is performed independently for the simplex and duplex data streams: operation of the simplex stream will be described with the understanding that identical operations are performed on the downstream data except at a different bit rate.

The DIA performs cyclic redundancy checks, data scramble/descrambler, Reed-Solomon endec functions, interleaving/de-interleaving, and data insertion and extraction for A/D functions and indicator bits.

Interfacing

The standard interface is a very straightforward buffered and demultiplexed synchronous connection. It is the same at both ATU-R and ATU-C, and presents four channels (simplex in and out, duplex in and out), with just two signals per connection, clock and data. (Obviously, the simplex in at ATU-R is not used). No framing signals are provided.

Table 6.   - Interface Descriptions

name	description
duplex_rx	**Duplex data output from the DTIR (ie data received)**
duplex_clko	**clock associated with duplex_rx (output)**
duplex_tx	**Duplex data input from the DTIR (ie data to be transmitted)**
duplex_clki	**clock associated with duplex_tx**
simplex_rx	**Simplex data output from the DTIR** **ATU-R: downstream data received** **ATU-C: not used**
simplex_clko	**clock associated with simplex_rx (output)**
simplex_tx	**Simplex data to be transmitted from the DTIR** **ATU-R: not used** **ATU-C: downstream data to be sent**
simplex_clki	**clock associated with simplex_tx (input)**

In general the tx clock signals (ie duplex_clocki, simplex_clki) are input to the DTIR, while the received data clock signals (duplex_clko, simplex_clko) are outputs. In other words, the sending modem (at ATU-C or ATU-R) supplies the clock to the DTIR, and the receiving modem's DTIR recovers it (using a digital phase locked loop) and supplies it to the external system. The channels all have separate - independent - clocks.

There is an exception to this; the recovered duplex_rx clock at the ATU-R can be used as duplex_clki for the duplex_tx data to be transmitted upstream. In this case the RT does not need a clock, as simplex and both duplex channels are clocked from the CO.

NB Although the DTIR includes much interfacing (eg elastic store, bit stuffing/robbing), it does not support the full suite of ASx and LSx multiplexing/demultiplexing. Instead, simple bit-synchronous data streams are provided. These essentially correspond to AS0 & LS0 but with variable rate, not merely fixed multiples of standard PDH rates, and with the optuion that the duplex LS0 can bne treated as two independent streams. The framing operation can then be defined by the system for their requirements, eg for V.35, ATM or 10BaseT.

Alternatively, for asynchronous access, the buffering multiplex/demultiplex and bit stuff/rob operations may be bypassed. These blocks are then power-downed, reducing the AD6435's power consumption. The interface presented is then a "raw" stream of upstream and downstream data, and the external system is responsible for framing. As the elastic store has been disabled, these have the relic of the ADSL line super-frame structure, and will show an irregular clock (with a pause for every 69th frame).

AD6436 DME

The DME consists of five major blocks, a QAM encoder/decoder block, an FFT block, an IFFT block, a DFIC block, and a control logic block.

The QAM block performs the constellation encoding and decoding required on each of the sub-carriers. It is shared by the TX and RX paths. These sub-carriers are then combined into a single stream for transmittal (more specifically, this is implemented by an inverse FFT which translates the frequency domain information of 255 separate subcarriers and combines it into a time domain sequence for transmittal). Conversely, the FFT block receives a sequence of received data, and separates it to give the sub-carriers for QAM demodulation. The IFFT block performs a 512 pt. inverse FFT in CO mode and a 64 pt. inverse FFT in RT mode on the transmit data.   The FFT block performs a 64 pt. FFT in CO mode and a 512 pt. FFT in RT mode. The FFT receives real data and produces complex conjugate symmetric data. In addition, the FFT block performs the FDQ operation on the data after the FFT is

completed.

ADTSP-2183

A versatile general-purpose 16-bit fixed point DSP with 80Kbytes of on-chip SRAM, the ADTSP-2183 is a 3.3V version of the ADSP-2181. It is used for training and synchronization tasks where programmability is important.   The DSP is also responsible for the AOC and EOC channels, which are inserted and extracted from the line data. This allows the processor to monitor or act on them, under program control.

It operates entirely from internal memory, with program being downloaded from a boot EPROM. Onchip there are 16Kwords of program memory, 16Kwords of data memory. All system RAM (except the 32K interleave memory) is internal.

The processor is most occupied during training and initialization, although it is regularly active overseeing operations, managing bit-swapping etc. As such, it can be used a general purpose control processor eg for OAM&P duties. Since the control is software based, there is considerable flexibility in configuration and management.

The modem is configured and managed by passing instructions to this processor through its serial port (SPORT1) or via the IDMA port.

Software (Configuration & Management)

In addition to the modem (datapump) software, a full control & management protocol stack (or API) is supplied with the chipset.

Configuration & management of the modem is implemented using a simple messaging protocol (MP). This allows a management entity -ME- (for example, this could be a dedicated system microcontroller or va serial line to a PC) to read from & write to a set of Configuration and Management Variables (CMVs) within the ADSL chipset. This MP/CMV pairing is similar to the SNMP/MIB combination commonly used for network management.

The ATU-C and ATU-R are controlled as one entity, generally from the WAN (ie from the CO). However, configuration & management may (and usually will) be different for each. All the CMVs are accessible at the ATU-C (ie all ATU-R data is passed up to the ATU-C). Security & authentication are also supported.

There are variables corresponding to control & set up information (eg to set the operating modes, the desired data rate or for remote reset); performance measurements and diagnostics (eg errored seconds log, attenuation and SNR measurements); status (eg modem serial number) and others. The functionality is a super-set of that defined in T1.413. It also implements full management of rate adaptivity and operating mode.

Full details of this protocol & the CMV structure are available.

ANALOG SECTION

The AD6437 implements virtually all the analog & mixed-signal operations required in an ADSL system, in a single IC (80PQFP). These include:

> Progammable Gain Amplifier (0-30dB gain, in 1dB steps)
> Anti-aliassing filters (4th order low pass)
> High-speed ADC (10MSPS, 12-bit resolution)
> High-performance DAC (14-bit, 35MSPS, current output)
> Reconstruction filters (4th order low pass)

Output buffer
References
Auxiliary DAC for control of VCXO (7bit)

All the internal sections of the AD6437 can be used or they may be individually bypassed, which allows for easy customization (eg bypassing the standard filters and using external discrete ones) or testing.

The configuration and control of the AD6437 is via a serial port and internal control registers. This is used to set the filter corners (eg for CO or RT mode), to set the PGA gain, to load data into the auxiliary DAC, to enable or bypass the various blocks, and to enable built-in test operations.

Two external dual opamps are also required to implement filters; these are supplied with the chipset (AD8042 high-pass filter and band-pass filter).

The transmitter output is delivered by the AD816 differential line driver through matched termination resistors and a 1:2 step up transformer. The AD816 includes two high-speed high-power amplifiers for the drive section, and two pop amps. These implement the receive path operations in the hybrid, and are designed to minimize noise and handle the large voltage levels arising at the line interface. The drivers are typically configured in a differential mode, delivering an output signal of up to +26dBm, with the low distortion required of a DMT driver. A discrete balance network that is optimized to match typical loop impedances is used to provide good hybrid cancellation.

A POTS Splitter is also required in the ADSL system to allow regular telephone service to coexist with the ADSL signals. Frequency Division Multiplexing is used to transmit both the ADSL signal and POTS on the same twisted pair line already installed for POTS (with the analog phone line in bin 0, below 4KHz and the ADSL data signal starting in bin 8 - above 30KHz). The POTS Splitter is located between the twisted pair and the ADSL modem to provide the necessary filtering to isolate one signal from the other and route then to their proper destinations (the lower frequencies are passed to the telephone, the high ones to the signal processing in the ADSL modem). The splitter must be designed so that the POTS signal is unaffected by power interrupts, and the ADSL data circuitry is unaffected by the high-voltages present on the telephone circuit. Specifications for the splitter depend on the operator (primarily, whether an active or passive design is required). As such, the splitter is not part of the chipset.

EXPECTED SYSTEM PERFORMANCE

The following table and curves summarize some performance expectations for the Gen. 2 chipset. These models have been tested & calibrated on Gen 1 and are believed to be representative.

These numbers show the achievable bit rate on given loops assuming a standard 6dB of margin, using true device accurate simulation (ie including quantization & non-ideal behavior in the ADC, DAC; transistor level performance of amplifiers, filters and drivers; modeled effects of the transmission line and bit-accurate, fixed-point/finite precision implementation details of the algorithm and software).

The performance curves are plotted for three noise conditions: AWGN only (at -140dBm); AWGN and ETSI Noise Model "A"; and AWGN with 20 HDSL crosstalkers.   However, they do not contain an allowance for implementation (eg board noise or harmonics from a switching PSU, manufacturing variation in the modems etc). Table 7 includes a variety of standard loops under different conditions (crosstalk, using the PIOTS band for data, etc) and provides a range - the simulated result and then a (lower) value with an allowance of a further 3dB degradation for system level implementation. This is a very conservative figure; experience shows the implementation losses to be significantly less than 3dB.

Note that, when crosstalk is included, it has a more dominant effect. Because the modem supports a rate-adaptive mode this may be less of a concern, but rates are provided for several representative environments.

Table 7. Achievable Bit Rates With Generation 2 Chipset

Test Loop	Margin dB	no xtalk w/ POTS	xtalk (1) w/ POTS	xtalk (2) w/ POTS	xtalk (1) no POTS	xtalk (2) no POTS
CSA (4)	6	730-810 7600-8500	580-665 7000-8000	410-490 5000-5900	690-790 7100-8100	540-650 4800-5700
CSA (6)	6	1020-1110 770-8650	680-780 7000-7900	405-500 5000-5800	800-910 7000-7900	500-620 5000-5800
CSA (7)	6	975-1060 5700-6600	730-810 5500-6400	480-580 4450-5300	860-980 5700-6600	630-750 4550-5400
15kft 24 AWG	6	800-880 3800-4400			600-720 3100-3700	
15 kft 26AWG	6	560-640 1400-1750	170-260 670-1000	20-60 20-130	180-280 660-790	25-105 30-140
T1.601 (7)	6	690-770 2240-2650	290-370 1475-1920	60-95 380-600	350-450 1500-1950	130-190 380-600
T1.601 (13)	6	680-760 2300-2800	275-350 1860-2350	55-100 700-1050	325-450 1875-2400	100-175 700-1100

The crosstalk cases are:
xtalk (1)10 ISDN
xtalk (2) 10HDSL

The loops contain no bridge taps. The bin allocation was 8-27 for upstream, 28-255 for downstream & standard overhead was included (ie these rates are payload). The hybrid matching circuit was optimized for 26 AWG, so the results for 24 AWG suffer echo and could be improved upon
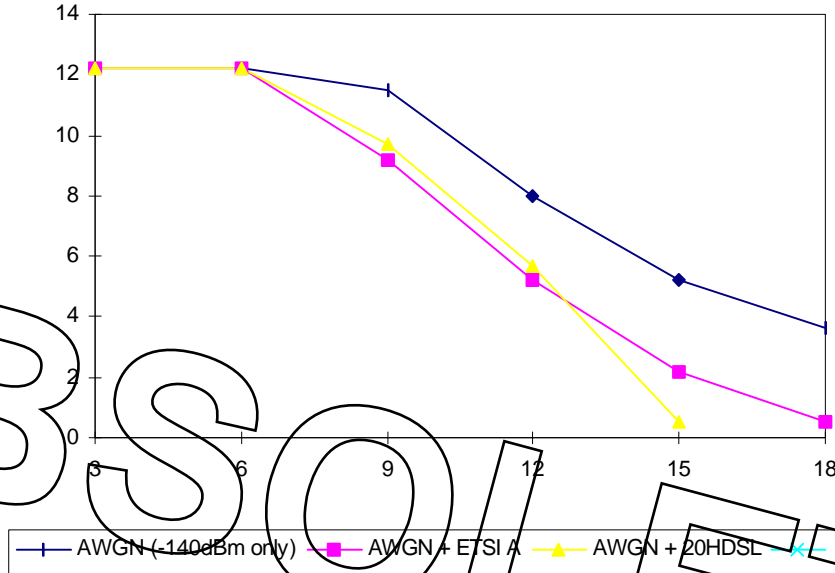.

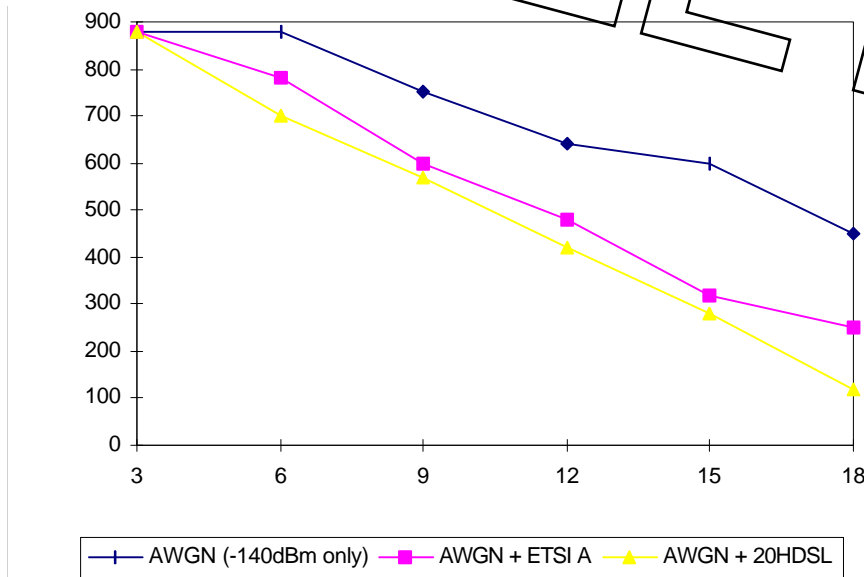**Figure 2. Downstream Data Rate vs Reach. 24AWG (0.5mm)**

Figure 3.   Upstream Data Rate vs Loop Reach. 24AWG (0.5mm)
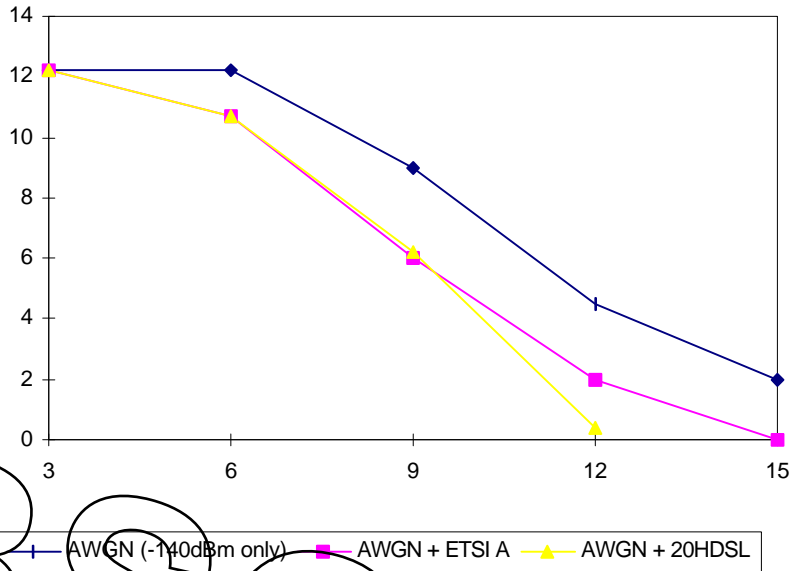
Figure 4. Downstream Data Rate vs Loop Reach. 26AWG (0.4mm)
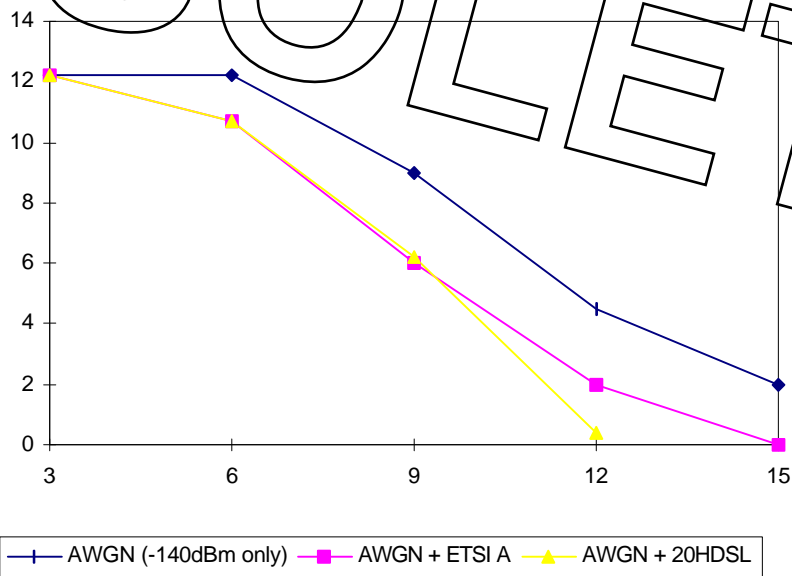
Figure 5. Upstream Data Rate vs Loop Reach. 26AWG (0.4mm)